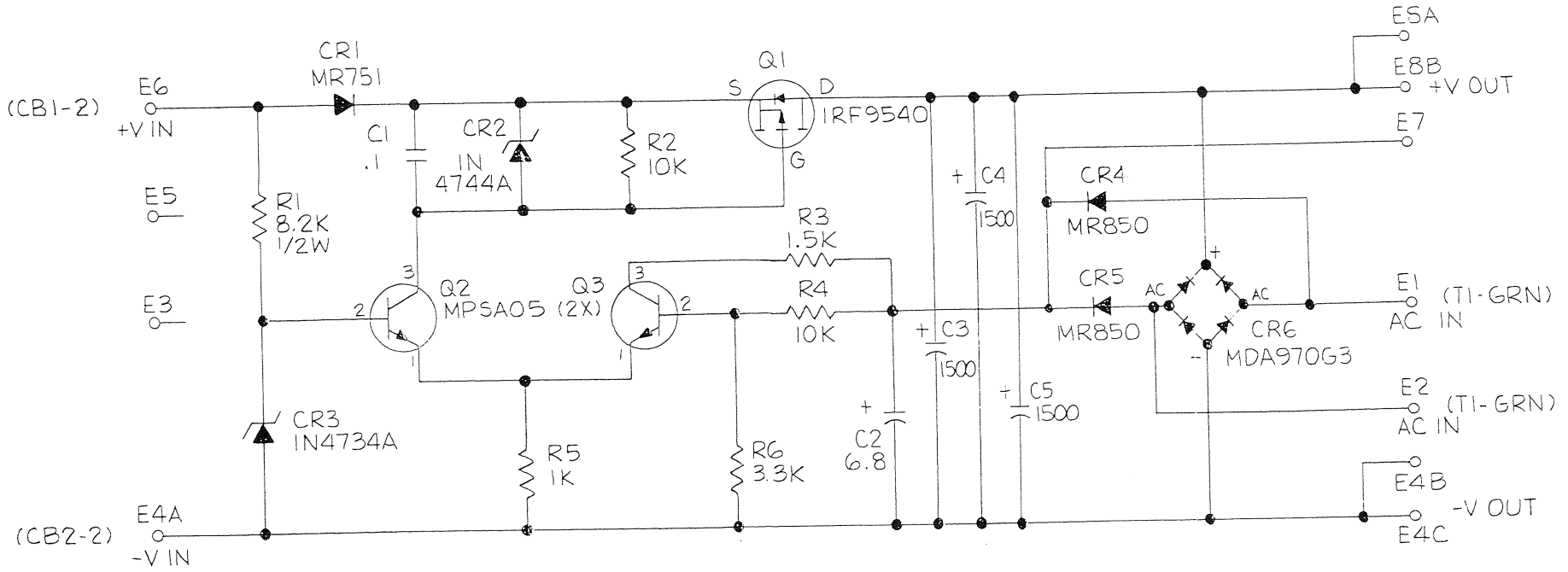
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	A	RELEASED	2/5/92	



2. ALL CAP VALUES ARE IN MICROFARADS.

1. ALL RESISTOR VALUES ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

10312479	GEN		
NEXT ASSY	USED ON	REF DES	FIG NO.
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

Q.A.	LOPEZ	2/18/92
ENGR	C.E.	3/6/92
CHECK	B. Hitzemann	2/5/92
DRAWN	[illegible]	1JUL91

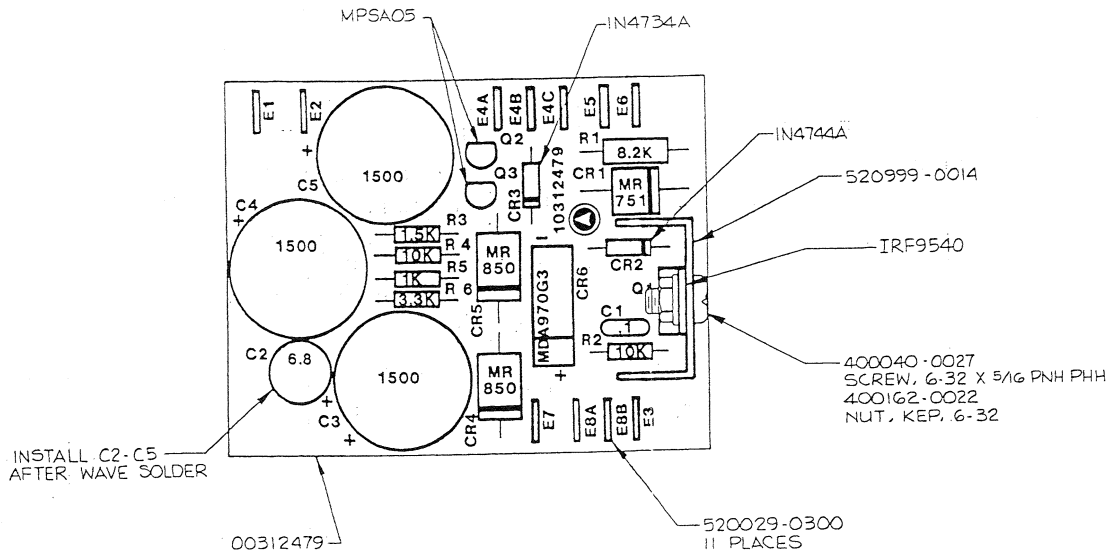
AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC,
AC/DC, +/-GND, POWER INPUT

SIZE	CODE IDENT NO.		REV
2	33 12	12312479	A

SCALE NONE SHEET 1 OF 1

ZONE	LTR	DESCRIPTION	DATE	APPD
	A	RELEASED	2/5/92	



	GEN		
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

Q.A.	Lotz	2-18-92
ENGR	CE	3Feb92
CHECKED	[signature]	2/5/92
DRAWN	[signature]	15JUL91

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY,
AC/DC, ±GND POWER INPUT

SIZE			
3	35	10312479	A

SCALE 2/1 SHEET 1 OF 1

1.4.3. Front Panel I/O (A1A2)

Reference Dwg. No. 12310754 and Dwg. No. 10310754

The Front Panel I/O assembly is the interface between the user and the instrument. Data is entered and receiver operation is modified through the keypad. Data and menu selections are displayed on the 4-line-40-character liquid crystal display.

The keys are connected to a key encoder IC (U3) in matrix fashion. When a key is pressed, the encoder debounces the closure and decodes a binary number representing that switch. This causes (U3,13) to go high, triggering the one-shot (U6), used as a latch here. IC (U6,9) goes low, producing an interrupt to the microprocessor on the Data Processor PCB. The microprocessor responds to the interrupt by reading the switch code from (U3) through buffer (U1). This clears (U3), enabling it for another closure.

The Data Processor interface to the LCD is on this board. Data lines D0 through D7 are connected to the LCD, along with control lines E1, E2, A1 and R/W. Using these signals, the Data Processor controls the LCD.

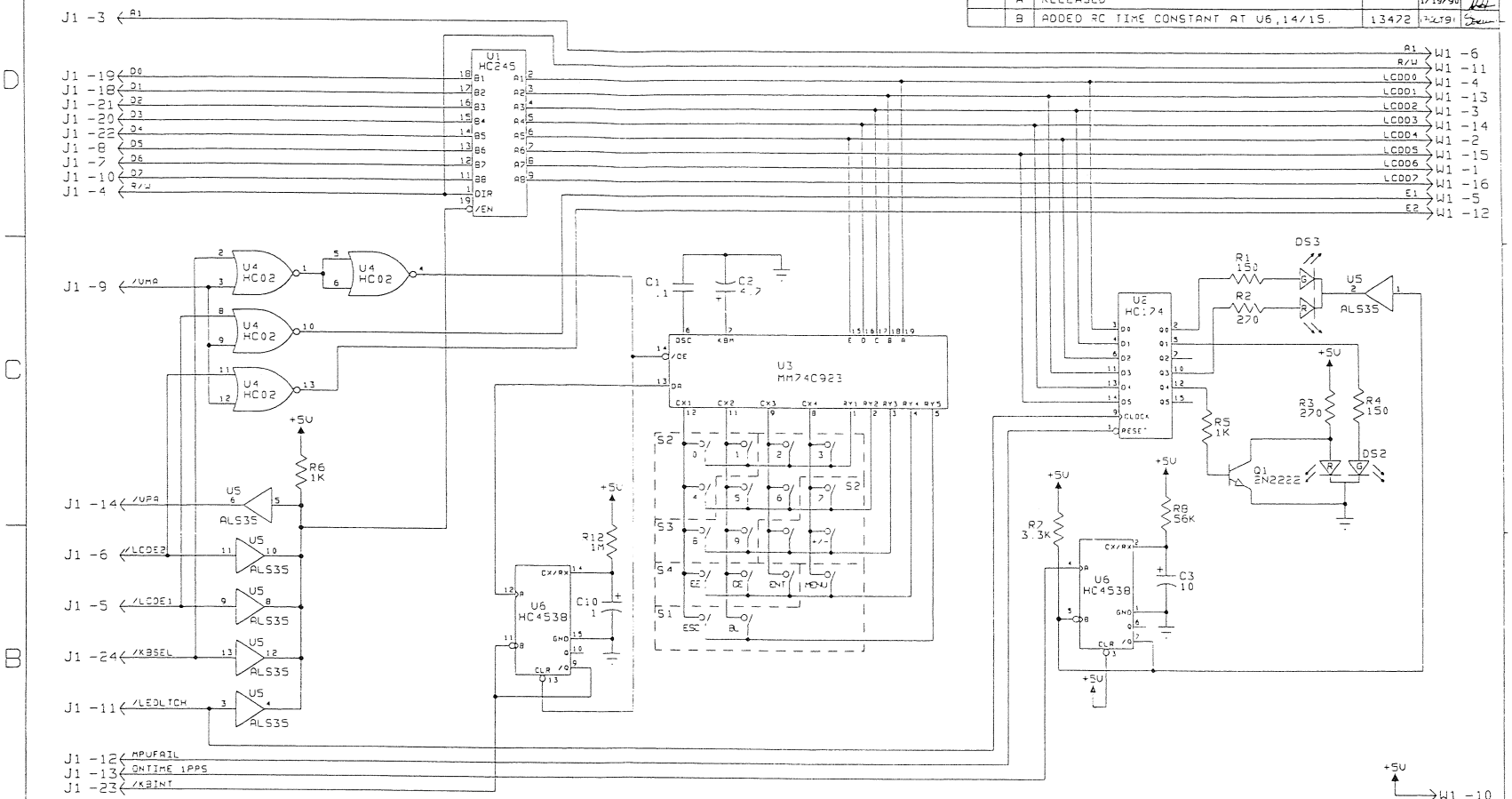
There are three two-color LEDs on the front panel, DS1, DS2 and DS3. Only the green half of DS1 is used, showing that the 5 volts is present. DS2 is the ALARM LED and DS3 is the 1 pps LED. These four LEDs (two pairs) are controlled by the Data Processor by writing data to latch (U2). The red and green LEDs of DS3 and the green LED of DS2 are turned on by setting the corresponding outputs of (U2) high. Because transistor, Q1, inverts the signal from (U2,12), the red LED of DS2 is turned on when (U2,12) is set low.

During normal operation, the Data Processor keeps the MR (memory reset) input of (U2) at a high level. If the microprocessor develops a problem, the MPUFAIL signal at J1-12 goes low, resetting (U2). This causes outputs Q0 through Q4 to go low, turning off both 1 pps LEDs and the green ALARM LED, and turning on the red ALARM LED. This gives a visual indication on the front panel that something is wrong with the instrument.

The on-time 1 pps, J1-13, triggers one-shot (U6). The output of (U5) is buffered by (U5), which has enough sink capability to turn on DS3. The period of (U6) is greater than 0.25 second, making it possible to see the LED when it lights.

NOTES:

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		1/19/90	
	B	ADDED RC TIME CONSTANT AT U6,14/15.	13472	7/27/91	



U6	16	8	C9
U5	14	7	C8
U4	14	7	C7
U3	20	10	C6
U2	16	8	C5
U1	20	10	C4
REF DES	VCC	GND	BYPASS CAP
PWR/GND CHART			

3. LAST DESIGNATORS USED: C10, CR1, DS3, J1, Q1, R12, S4, U6, W1.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

10310754	2201	1A1A2	
10310754	2200	1A1A2	
NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED
DO NOT SCALE THIS DRAWING
DECIMAL ± | FRACTIONAL ± | ANGULAR ±
MATERIAL

DRAFTER DanW 6/30/89
CHECKED Gulowski 1/9/90
ENGINEER JR Howell 1/8/90
Q.C. Lupet 1-15-90

AUSTRON INC a DATUM company

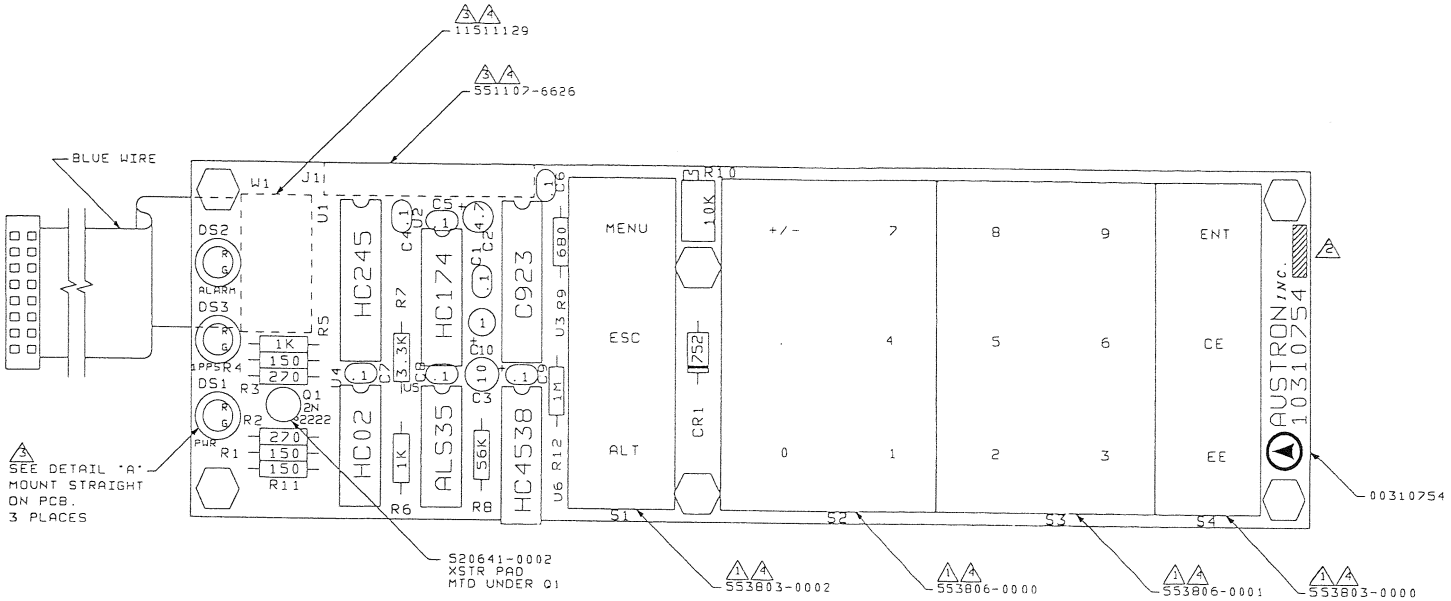
TITLE
SCHEMATIC,
FRONT PANEL I/O

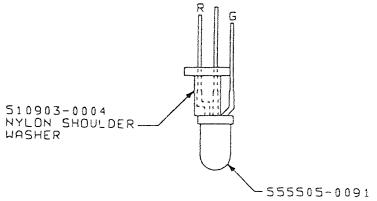
SIZE 3 | 39 | DRAWING NUMBER 12310754 | REVISION B
SCALE NONE | CAD GENERATED | Sheet 1 of 1

D C B A

8 7 6 5 4 3 2 1

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		1/19/90	
	B	BLU WIRE WAS BRN, ADDED XSTR PAD JFM	12966	5/7/90	
	C	ADDED C10 & R12 DonW	13472	7OCT91	
	D	REVISED PER ECO 13612		1/31/92	





DETAIL "A"
(NOT TO SCALE)

NOTES:

4. MOUNT FLUSH WITH PCB.
3. INSTALL AFTER WAVE SOLDER AND HAND SOLDER.
2. STAMP REVISION LETTER OF THIS DRAWING IN THE AREA SHOWN.
1. DO NOT WAVE SOLDER OR VAPOR CLEAN, HAND SOLDER & CLEAN WITH ALCOHOL ONLY.

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
10911944	2201	1A1A2	
10911118	2200	1A1A2	
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED
DO NOT SCALE THIS DRAWING
DECIMAL ± FRACTIONAL ± ANGULAR ±
MATERIAL
DRAWN DonW 7/6/89
CHECKED Bulowski 8/7/90
ENGINEER JR Bowell 8/9/90
P.C. Lopez 8/9/90

AUSTRON INC
A DATUM company

TITLE
PCB ASSY, FRONT PANEL I/O

SIZE 3 | 41 | DRAWING NUMBER 10310754 | REVISION D
SCALE 2:1 | CAD GENERATED | Sheet: 1 of: 1

1.4.4. Oscillator Control Card

Reference Dwg. No. 12312676 and Dwg. No. 10312676

The Oscillator Control Card is composed of five major circuits. The circuits are: oscillator control, oscillator output, frequency measurement, fault detection and temperature measurement. All microprocessor control is performed through address decoding in the LCA (Logic Cell Array) (U4) and data bus buffering by (U1) and (U2). The LCA is configured by the serial PROM (U3). The oscillator is connected to the Oscillator Control Card by a cable at J1. Power is supplied to the oscillator by selecting 24 Vdc or 15 Vdc with W2. The oscillator is either an ovenized voltage controlled crystal oscillator or a rubidium oscillator. The Oscillator Control Card identification S1 is set according to the following table.

The oscillator type selection is set at the factory. If the oscillator is being changed to a different type, this section describes the hardware setting changes necessary. The oscillator is either an ovenized voltage controlled crystal oscillator or a rubidium oscillator. The oscillator type is set on the control card identification switch S1 according to the following table.

Table 1: Osc. Control Card Select Settings

Oscillator	ID Code	S1-1	S1-2	S1-3	S1-4	W1	W2	R3
*1121←	(00)	0	0	0	0	2-3	1-2	INSTL
1120L	01	1	0	0	0	1-2	1-2	INSTL
1180	02	0	1	0	0	1-2	1-2	INSTL
Rb FRS	08	0	0	0	1	1-2	2-3	OPEN
Rb FRK	09	1	0	0	1	1-2	2-3	OPEN

* is the only configuration offered in Model 2201A.

Oscillator control is achieved by the D/A converter (U6). The D/A converter receives control voltage information over the data bus and provides the control voltage as electronic tuning (ET) to the oscillator.

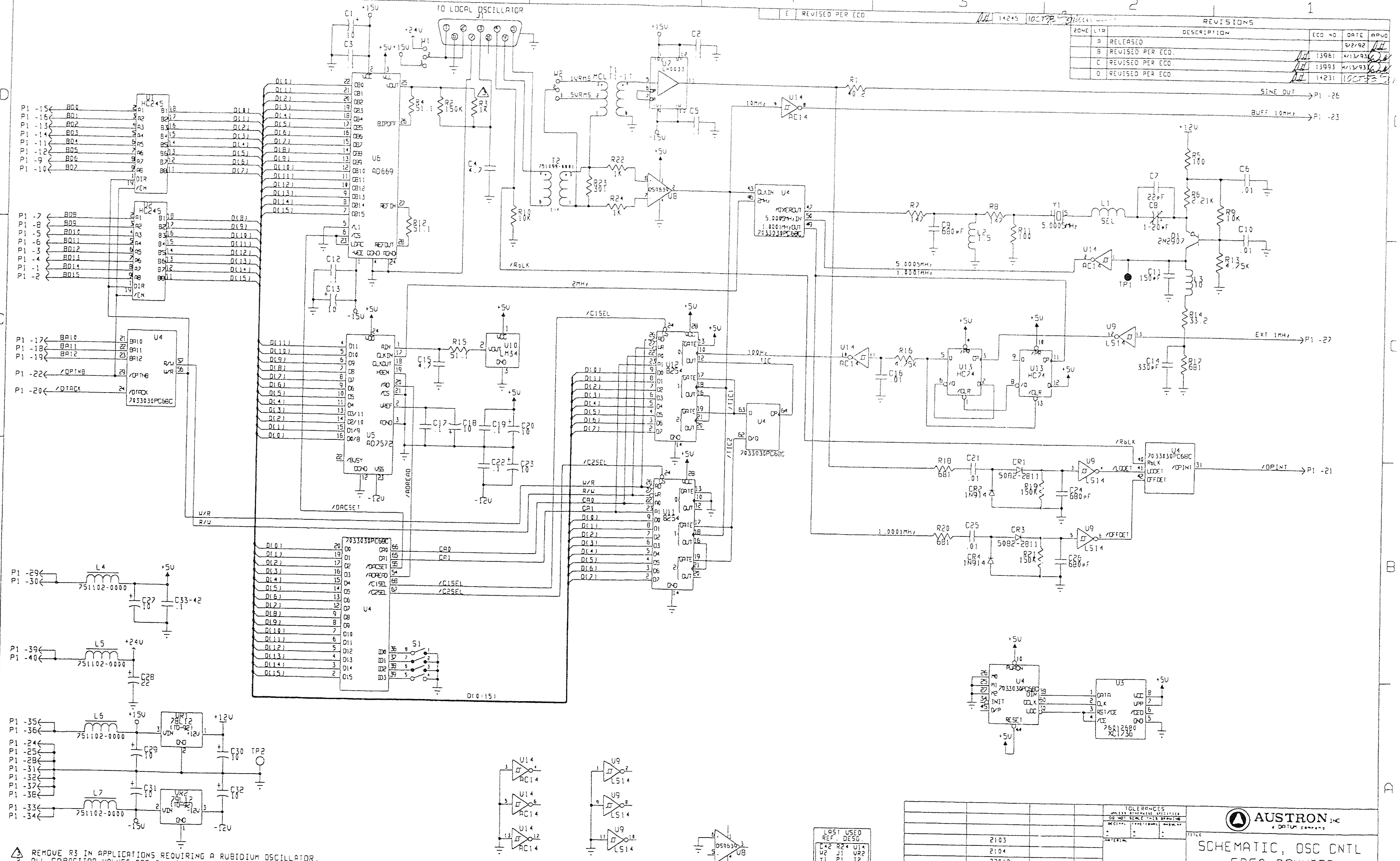
Oscillator output is available as 10 MHz sine wave output and buffered square wave. The jumper W1 is set for 1 Vrms or 0.5 Vrms oscillator output level to always provide 1 Vrms through sine out. Sine wave output is driven by the buffer (U7). The 10 MHz square wave is achieved by hard limiting the oscillator output with (U8), then driving an advanced CMOS gate in (U9) for the buffered output.

The frequency measurement circuit consist of an offset frequency generator, phase detector and time interval counters. An offset frequency is generated by mixing 5 MHz and 500 Hz in the LCA (U4), then filtering off 5.0005 MHz using the crystal filter circuit that includes Y1 and Q1. The 5.0005 MHz is divided to 1.0001 MHz in (U4) and phase mixed in (U13) with the external reference 1 MHz. The phase detector (U13) output is filtered by R15, C15 and (U9) to provide 100 Hz + Δf_{REF}. The 100 Hz + Δf_{REF} clocks counter 0 of (U12) for a one second time interval output. The one second time intervals are alternately measured by the rest of (U12) and (U11) being clocked by the buffered 10 MHz. These one second interval counts with 10 MHz resolution provide phase information for the measurement of the external reference frequency.

The fault detection circuit includes detecting loss of oscillator output, loss of offset frequency output and loss of rubidium oscillator lock (when applicable). Detection of the oscillator output and offset frequency output involves rectifying and filtering each output, then detecting the resulting high level with gates in (U9). Each detected output from the gates in (U9) and the rubidium oscillator lock signal are combined in (U4) to provide the oscillator card option interrupt and fault detection status.

The temperature measurement circuit consist of the temperature sensor (U10) and the A/D converter (U5). Temperature is regularly read over the data bus for temperature compensation applications.

REV: E



ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		9/2/92	
	B	REVISED PER ECO.	13961	4/13/93	
	C	REVISED PER ECO.	13993	4/13/93	
	D	REVISED PER ECO.	14231	10CT93	
	E	REVISED PER ECO.	14245	10CT93	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 1%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. REMOVE R3 IN APPLICATIONS REQUIRING A RUBIDIUM OSCILLATOR.

LAST USED REF. DESG.		
C42	R24	U14
W2	J1	VR2
Y1	P1	T2
L7	CR4	S1
Q1	TP2	

NEXT ASSY	USED ON
	2103
	2104
	2201A
	2200A&B

APPLICATION

AUSTRON INC — A DATUM COMPANY

SCHEMATIC, OSC CNTL FREQ COUNTER

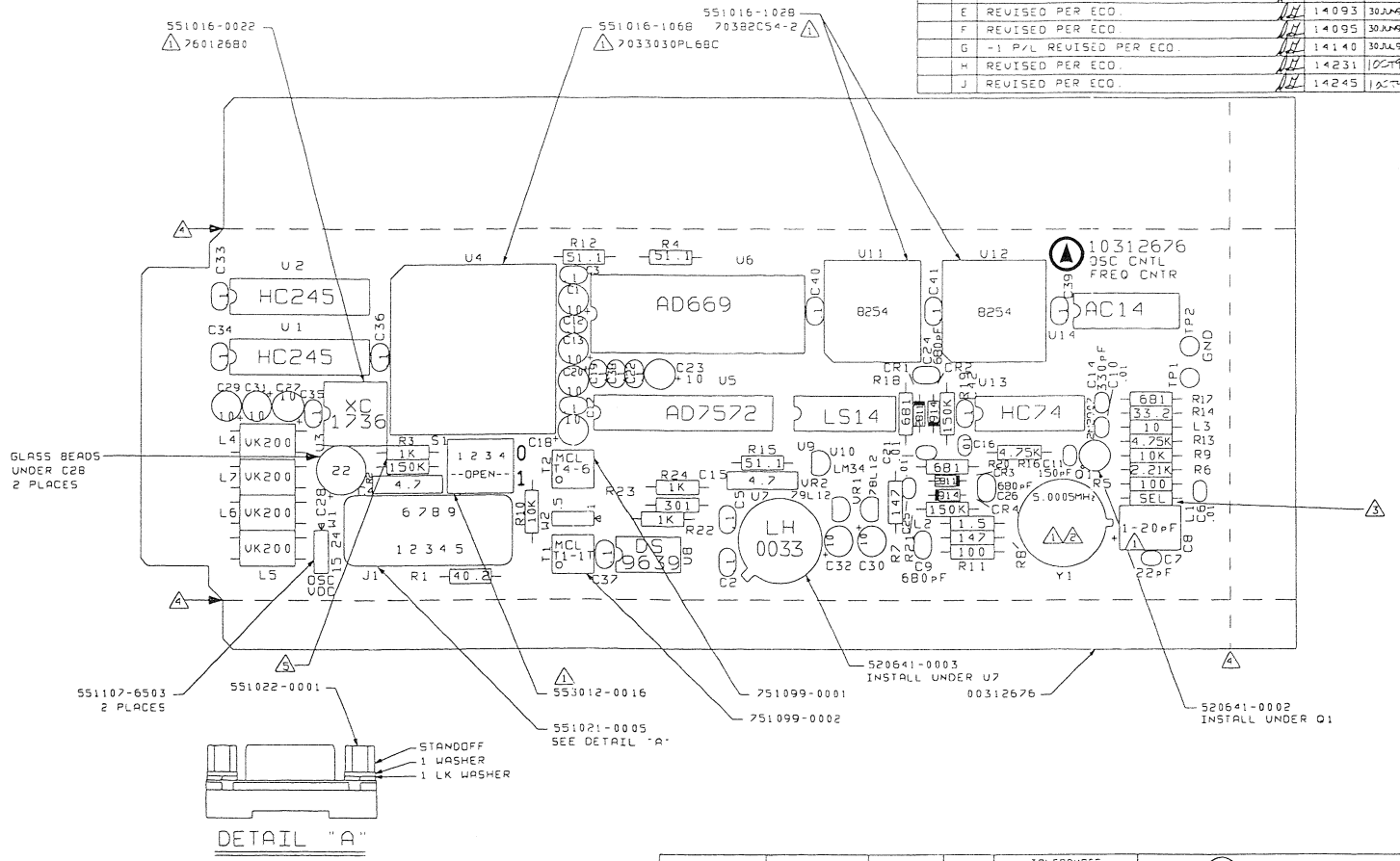
DRAWN D. DUTKOWSKI 9/2/92
J. LOPEZ 9/2/92

DRAWING NUMBER 12312676 REV E

CAD GENERATED — SHEET 1 of 1

45

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		9/2/92	
	B	REVISED PER ECO.	13961	4/13/93	
	C	REVISED PER ECO.	13977	4/13/93	
	D	REVISED PER ECO.	13993	4/13/93	
	E	REVISED PER ECO.	14093	30JUN93	
	F	REVISED PER ECO.	14095	30JUN93	
	G	-1 P/L REVISED PER ECO.	14140	30JUL93	
	H	REVISED PER ECO.	14231	10CT93	
	J	REVISED PER ECO.	14245	10CT93	



5. REMOVE R3 IN APPLICATIONS REQUIRING A RUBIDIUM OSCILLATOR.
4. WHEN -1 IS REQUIRED, BREAK OFF EDGES AT BREAK POINTS.
3. INSTALL A 22AWG WIRE JUMPER IN PLACE OF SELECT INDUCTOR L1.
2. DO NOT PREP CRYSTAL Y1 LEADS.
1. INSTALL AFTER WAVE SOLDER & VAPOR DEGREASE.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
	2104		
	2103		
	2201		
	2200		
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED
DO NOT SCALE THIS DRAWING
DECIMAL ± | FRACTIONAL ± | ANGULAR ±

MATERIAL

DRAWN [signature] DATE 4/29/92
CHECKED D. GUTOWSKI DATE 9/2/92
CHECKED CE DATE 9/2/92
STD J. LOPEZ DATE 9/2/92

AUSTRON INC
A DATUM COMPANY

TITLE
PCB ASSY, OSC CNTL
FREQ COUNTER

SIZE 3 | SCALE 1:1 | DRAWING NUMBER 10312676 * | REVISION J
CAD GENERATED | Sheet 1 of 1

1.4.5. Data Processor

Reference Dwg. No. 12312798 and Dwg. No. 10312798

The Data Processor consists of a 68010 microprocessor (U18), 512 Kbytes of EPROM [(U14), (U15), (U30) and (U31)], 256 Kbytes of static RAM [(U50) and (U51)], 4 Kbytes of battery-backed RAM [(U13) and (U29)], a time-interval-counter (sheet 2 of schematic), interrupt processing circuitry and various interface ICs.

The heart of the Data Processor PCB is the 68010 microprocessor. It is a 16-bit MPU, with 32-bit internal operations. Data reads and data writes are handled asynchronously. That is, when a data access is begun, the microprocessor waits until either $\overline{\text{DTACK}}$ or $\overline{\text{VPA}}$ is pulled active low, indicating that the device being accessed is ready to give or take data. This allows slow devices time to respond. When the device is ready, it asserts $\overline{\text{DTACK}}$ or $\overline{\text{VPA}}$, allowing the microprocessor to complete the access.

When power is applied, the power detect circuit (U11) forces the Reset and Halt inputs to the MPU low for at least 0.25 second after the 5 volts passes 4 volts. This causes a general reset of the MPU. At the end of the delay, the Reset and Halt lines go high, allowing the MPU to function normally. During normal operation of the receiver, (U11) monitors the 5 volt line. If it ever drops below approximately 4 volts, (U11) generates a Reset and Halt to the microprocessor. Within 0.25 second of the 5 volt line returning to normal, (U11) sets Reset and Halt high, resuming normal operation. This prevents activity when the 5 volt power is low enough to cause improper operation.

The MPU clock is derived from the 20 MHz oscillator (U2) by dividing it by two in (U1). This 10 MHz clock provides the necessary timing for instruction execution.

The MPU address and data lines are connected to the four EPROM ICs, which are organized as 256 K words. Contained within the EPROMs is the software which controls the instrument. In the simplest terms, the microprocessor removes an instruction from the EPROMs, determines what the instruction is, then performs that instruction. When it is through, it takes another instruction and continues. $\overline{\text{PROM1}}$ and $\overline{\text{PROM2}}$ are the enable signals for the EPROMs, and are generated by (U17).

The static RAM is organized as 128 K words, but each byte can be accessed separately, giving 256 K individual bytes. Static RAM ICs (U50) and (U51) make up this RAM with (U50) being on the even byte boundaries and (U51) on the odd. They are selected with the $\overline{\text{RAM1H}}$ and $\overline{\text{RAM1L}}$ signals generated by (U17).

The battery-backed memory is organized as 4 Kbytes. It consists of two, 2 Kbyte RAM ICs, each with its own internal battery. (U29) and (U13) are identical in pinout and have the same capacity, but (U13) includes a real-time-clock. This clock continues to function while the main power is off, eliminating the need to reset time-of-day and date every time power is restored. The data stored within these RAMs is also retained while power is off.

ICs (U16), (U17) and (U32), are specially programmed ICs that decode the address lines to produce the strobes necessary for the MPU to access the hardware. Each IC produces its own set of strobes, controlling particular parts of the hardware. On the schematic, the inputs for these ICs are shown on the left and the outputs on the right.

IC (U46) is a specially programmed IC that controls the interrupts in the receiver. There are seven priority levels of interrupts on the Data Processor. The highest level is $\overline{\text{INT7}}$ (U46,2) and the lowest is $\overline{\text{INT1}}$ (U46,8). IC (U46) monitors these seven interrupts. When one occurs, it assigns the interrupt a 3-bit code and outputs it to the microprocessor on $\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$ and $\overline{\text{IPL2}}$.

When the microprocessor recognizes this interrupt, it responds by setting FC0, FC1,and FC2 high. IC (U46) then completes the handshake by pulling $\overline{A}$ low. When the software that services that interrupt is run, the interrupt is cleared and $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$ and $\overline{VPA}$ go inactive high. If a second interrupt occurs at the same time as the first, and if it has a higher priority, the 3-bit code of the second interrupt is sent to the microprocessor, even though the first has not been serviced. If a second interrupt of lower priority occurs, its code will not be placed on the bus until the higher priority interrupt has been cleared.

Shift register (U43) is a watchdog timer, that monitors the microprocessor $\overline{AS}$ line for abnormal operation. When $\overline{AS}$ goes low, $\overline{PL}$ goes high and (U43) begins clocking a logic one through its eight flip-flops, at a 1.0 MHz rate. If the $\overline{AS}$ line has not returned high by the eighth clock pulse (after 8 microseconds) output $\overline{QH}$ goes low, causing a bus error ($\overline{BERR}$). The microprocessor responds in a fashion appropriate for the time of occurrence. If $\overline{AS}$ goes high in less than 8 microseconds (it usually goes high within 275 nanoseconds) $\overline{BERR}$ is not generated.

Decoder IC (U9) decodes address lines A13, A14 and A15, along with the $\overline{OPTIONS}$ strobe, to generate the select strobes for the option slots. One strobe goes to each of the plug-in slots on the rear panel, except for slot A8 (Antenna Interface module). The eighth strobe goes to the Oscillator slot.

ICs (U3), (U4), (U5) and (U8) buffer the 23 address lines and various microprocessor control lines, before they are connected to PCB edge-connector P1. ICs (U6) and (U7) buffer the 16 data lines.

On sheet 2 of the Data Processor schematic you will find the schematic of the time interval counter. The microprocessor controls the operation of this circuit and processes the output. A discussion of the operation of this circuit follows.

In normal operation, the microprocessor sets the two flip-flops in (U45) to 0 (U45,5) and 0 (U45,9), which determine the YA and YB outputs of multiplexer (U10). This causes the time interval counter to start on the occurrence of the Internal 1 pps (YA output) and stop on the next occurrence of the External 1 pps (YB output).

When the START pulse occurs, (U49,9) goes high, enabling the STOP input [other half of (U49)]. At the same time, (U49,8) goes low, starting integrator (U27) ramping from a slightly negative level in a positive direction. On the first rising edge of the 5 MHz clock, the QA output of shift register (U48) goes high. This results in the output of NAND gate (U47,11) going low, enabling counters 1 and 2 in (U19). As long as (U19,4) is high, this 32- bit counter counts the 5 MHz clock.

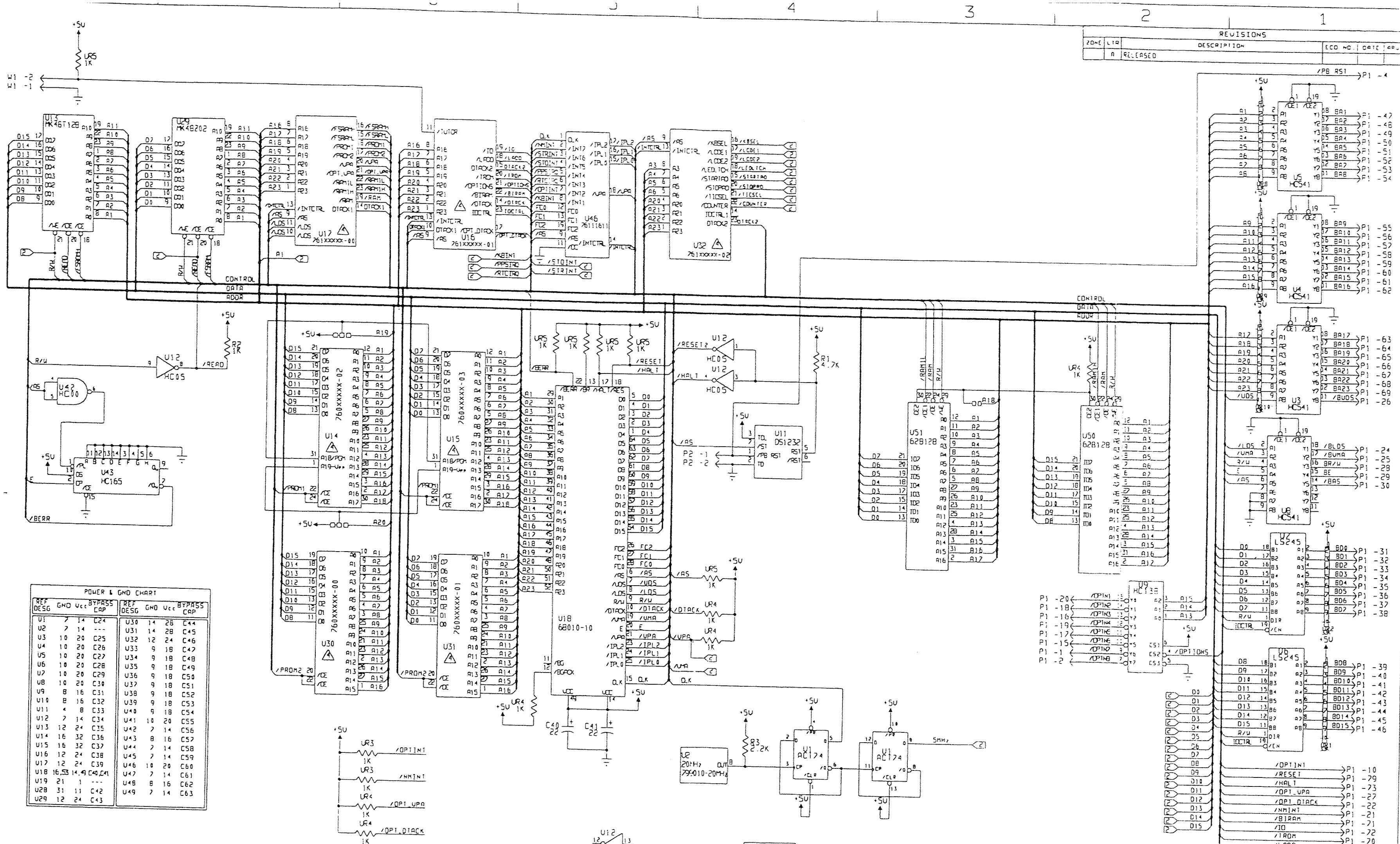
On the second rising edge of the 5 MHz clock after the start pulse, output QB of (U48) goes high. This causes track-and-hold (U26) to go into the hold state, saving the current value of the voltage ramp from integrator (U27). On the fourth rising edge of the 5 MHz clock, output QD of (U48) goes high, clocking (U44). IC (U44,8) goes low, generating an interrupt to the microprocessor. The microprocessor responds to this interrupt by strobing A/D converter (U25) causing it to begin converting the voltage saved in (U26).

When the STOP pulse occurs, (U49,6) goes low, starting integrator (U22) ramping from a slightly negative level, in a positive direction.On the second rising edge of the 5 MHz clock, the QB output (pin 12) of shift register (U48) goes high, putting track/hold (U21) in the hold state, saving the current value of the voltage ramp from integrator (U22). At the same time, (U47,6) goes low and (U47,11) goes high, stopping counter (U19). When the fourth rising edge of the 5 MHz clock occurs, the QD output of (U48) pin 2 goes high, causing an interrupt. The

microprocessor responds to this interrupt by strobing A/D converter (U20) causing it to begin converting the voltage saved in (U21).

After a short delay, the microprocessor reads the contents of (U25) and (U20), and the contents of counters 1 and 2 in (U19). This data is then processed by the microprocessor to get the time interval between the two pulses. As soon as that is completed, a new cycle can begin.

NOTES:



POWER & GND CHART							
REF DESG	GND	Vcc	BYPASS CAP	REF DESG	GND	Vcc	BYPASS CAP
U1	7	14	C24	U30	14	28	C44
U2	7	14	---	U31	14	28	C45
U3	10	20	C25	U32	12	24	C46
U4	10	20	C26	U33	9	18	C47
U5	10	20	C27	U34	9	18	C48
U6	10	20	C28	U35	9	18	C49
U7	10	20	C29	U36	9	18	C50
U8	10	20	C30	U37	9	18	C51
U9	8	16	C31	U38	9	18	C52
U10	8	16	C32	U39	9	18	C53
U11	4	8	C33	U40	9	18	C54
U12	7	14	C34	U41	10	20	C55
U13	12	24	C35	U42	7	14	C56
U14	16	32	C36	U43	8	16	C57
U15	16	32	C37	U44	7	14	C58
U16	12	24	C38	U45	7	14	C59
U17	12	24	C39	U46	10	20	C60
U18	16,53	14,49	C40,C41	U47	7	14	C61
U19	21	1	---	U48	8	16	C62
U28	31	11	C42	U49	7	14	C63
U29	12	24	C43				

LAST USED REF. DES.	
R21	C65
CR4	U49
P2	J1
W6	

4. SEE MODEL NO. TABLE ON ASSY DWG FOR PROPER EPROM & PAL SET.
3. JUMPERS W1 & P2 ARE OPEN FOR NORMAL OPERATION.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
10312798	2201	1A2A2	
10312798	2200	1A2A2	

APPLICATION

TOLERANCES

DO NOT SCALE THIS DRAWING

AUSTRON INC
a DATUM company

SCHEMATIC, ENHANCED DATA PROCESSOR

53

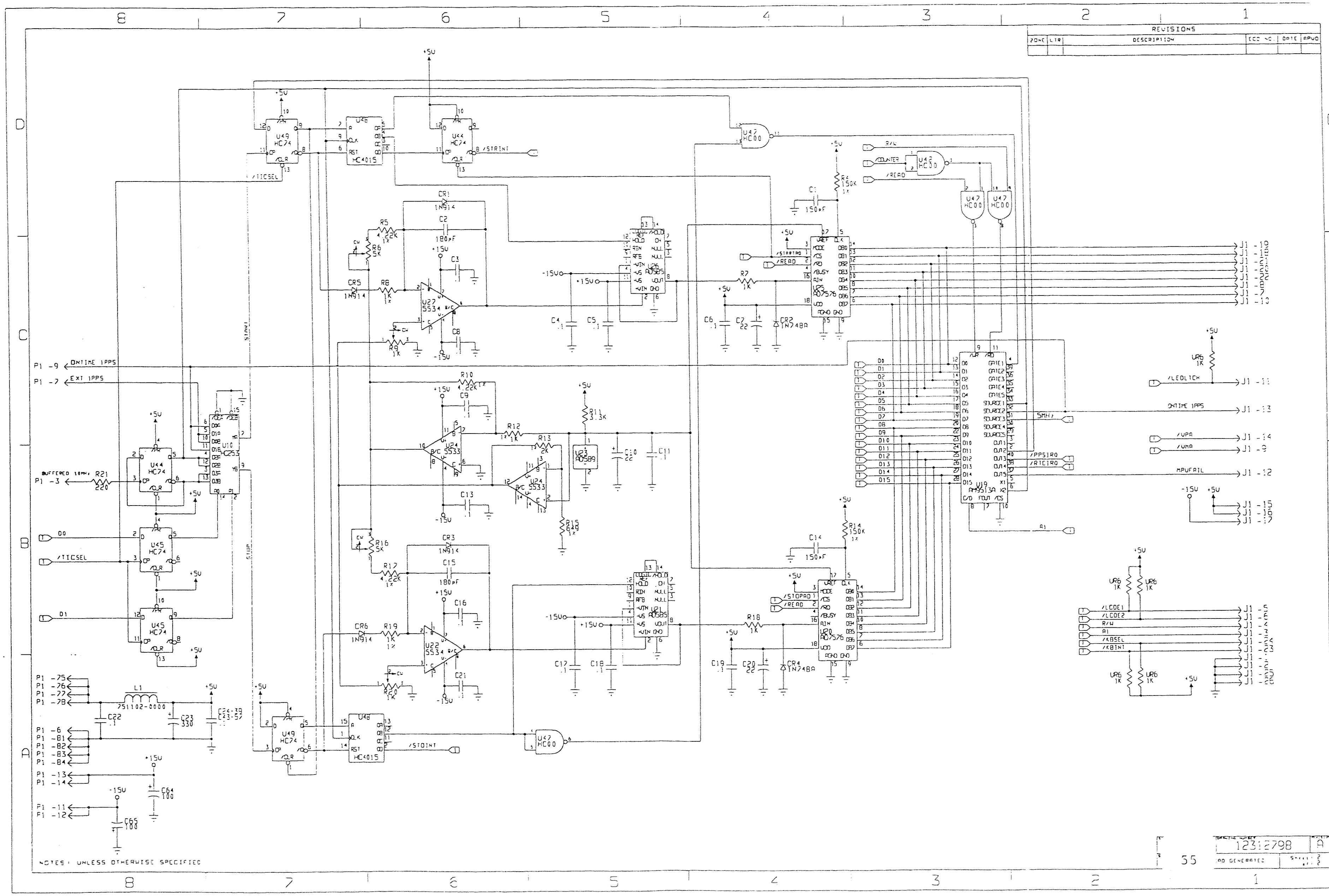
12312798 A

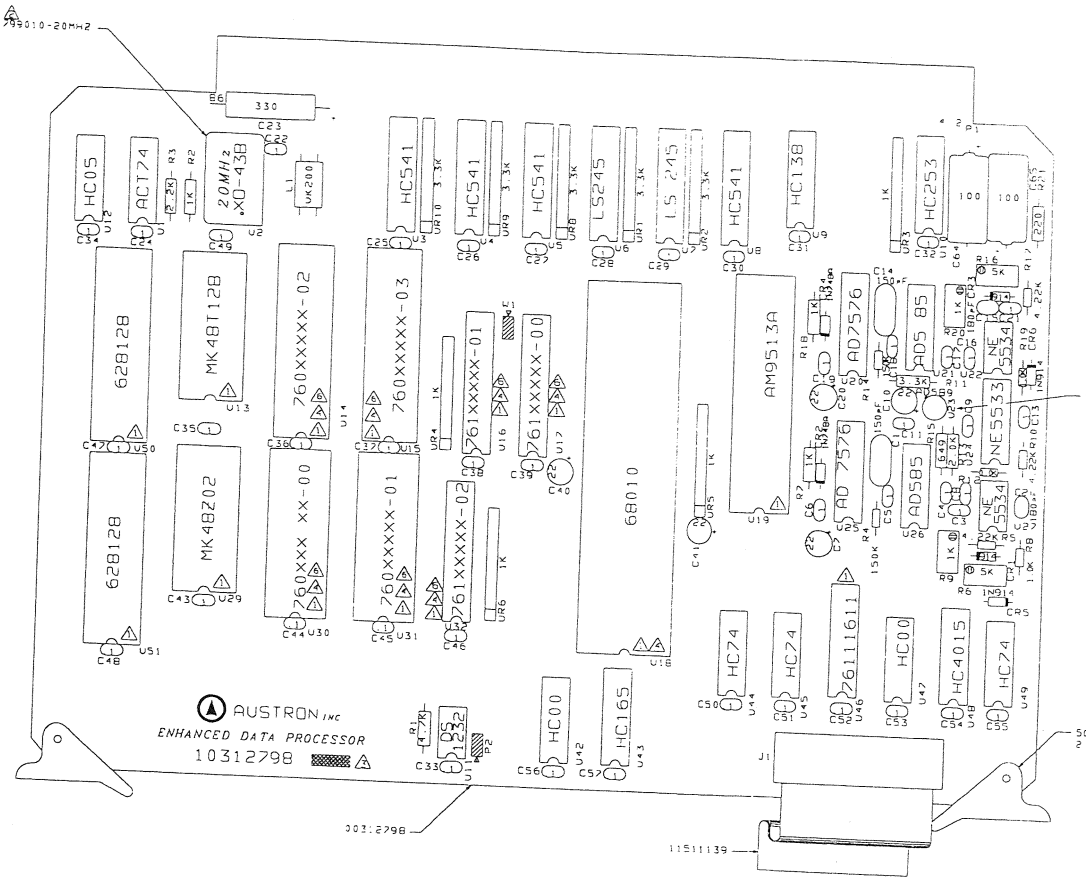
CAD GENERATED

Sheet 1 of 2

REVISIONS

ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APPD
	A	RELEASED			


REVISIONS
ZONE
LTR
DESCRIPTION
ECO NO
DATE
APVD
NOTES: UNLESS OTHERWISE SPECIFIED
12312798
A
55



SOCKET LOCATION TABLE

SOCKETS USED ON		
REF	PART NUMBER	SIZE
U19	551016-0003	40
U13 U29	551016-0004	24
U14 U15	551016-0024	32
U30 U31	551016-0009	28
U18	551016-0035	64
U16 U17 U32	551017-0024	24
U50 U51	551016-0029	32
U46	551015-9900	20

MODEL NO. TABLE

MODEL	PAL SET	U16	U17	U32	EPROM SET	U14	U15	U33	U31
2200	76110816	-01	-00	-02	76010812	-02	-03	-00	-01
2200A	76112793	-01	-00	-02	76012772	-02	-03	N/U	N/U
2201	76110816	-01	-00	-02	76011954	-02	-03	-00	-01
2201A	76112793	-01	-00	-02	76012781	-02	-03	N/U	N/U
2105	76112793	-01	-00	-02	76012751	-02	-03	N/U	N/U
2101	76112793	-01	-00	-02	76012687	-02	-03	N/U	N/U
2103	76112793	-01	-00	-02	76012797	-02	-03	N/U	N/U
2202	76112793	-01	-00	-02	76012542	-02	-03	N/U	N/U

* N/U = NOT USED

1. SEE MODEL NO. TABLE FOR PROPER EPROM & PAL SET.
2. ▨ INDICATES PART NOT INSTALLED ON PCB.
3. THESE IC's ARE INSTALLED AT TEST LEVEL BY THE TEST DEPT.
4. STAMP REVISION LEVEL OF THIS DWG. WHERE SHOWN.
5. INSURE ALL SOCKETS & CONNECTORS ARE MOUNTED FLUSH TO PCB.
6. WAVE SOLDER IC SOCKETS ONLY. INSTALL IC's AFTER WAVE SOLDER. REFER TO SOCKET LOCATION TABLE BEFORE INSTALLING SOCKETS.

NOTE:

REVISIONS				
ZONE	LTR	DESCRIPTION	ECO NO.	DATE
	A	RELEASED		

PART NUMBER	QTY	REFERENCE DESIGNATION	FIGURE NUMBER
25412245	2210	1:3105	
25412245	2105	10105	
25412682	2104	10202	
25411941	2201/A	10202	
25410922	2201/A	13202	

NEXT ASSY | USED ON | APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED

AUSTRON INC

TITLE: PCB ASSY, ENHANCED DATA PROCESSOR

10312798 A

SHEET 1 OF 1

57

1.4.6. Signal Controller (A2A3)

Reference Dwg. No. 12310952 and Dwg. No. 10310952

The Signal Controller is responsible for acquiring and tracking the satellites. It also controls the hardware that produces the 1 pps. It consists of a 68010 microprocessor, 16 Kbytes of EPROM, 4 Kbytes of dual port RAM and the C/A code generator. In addition to controlling all of the Signal Processor hardware, it takes commands from the Data Processor and sends satellite data to the Data Processor, via the dual port RAM.

The heart of the Signal Controller PCB is the 68010 microprocessor. It is a 16-bit MPU, with 32-bit internal operations. Data reads and data writes are handled asynchronously. That is, when a data access is begun, the microprocessor waits until either $\overline{\text{DTACK}}$ or $\overline{\text{VPA}}$ is pulled active low, indicating that the device being accessed is ready to give or take data. This allows slow devices time to respond. When the device is ready, it asserts $\overline{\text{DTACK}}$ or $\overline{\text{VPA}}$, allowing the microprocessor to complete the access.

When power is turned on, (U13) sets its output, pin 5, high for at least 0.25 second. This pulls the Reset and Halt inputs of the microprocessor low, producing a general reset. After the delay, (U13,5) goes low and the microprocessor begins to function normally. During normal operation of the receiver, (U13) monitors the 5 volt line. If it ever drops below approximately 4 volts, (U13) generates a Reset and Halt to the microprocessor. Within 0.25 second of the 5 volt line returning to normal, (U13) sets Reset and Halt high, resuming normal operation. This prevents activity when the 5 volt power is low enough to cause improper operation.

The microprocessor clock is derived from the 20 MHz oscillator (U8) by dividing it by two in (U9). This 10 MHz clock provides the necessary timing for instruction execution.

The microprocessor address and data lines are connected to the two EPROM ICs, which are organized as eight K words. Contained within the EPROMs is the software which controls the instrument. In the simplest terms, the microprocessor removes an instruction from the EPROMs, determines what the instruction is, then performs that instruction. When it is through, it takes another instruction and continues. ROMU and ROML are the enable signals for the EPROMs, and are generated by (U21).

The dual port RAM is organized as 4 Kbytes of RAM, consisting of two 2 Kbyte dual port RAMs, (U6) and (U7). ICs (U6) and (U7) are similar, but (U7) is subordinate to (U6). When the RAM is selected by both microprocessors, (U6) determines which microprocessor must wait. It then pulls the appropriate BUSY output low (asserted). The BUSY input of (U7) is connected to this same signal and responds the same as (U6). When the other microprocessor has finished its access of the RAM, the BUSY line goes high, allowing the delayed microprocessor to finish its access. This prevents problems when both microprocessors attempt to access the same location in the RAM ICs at the same time.

IC (U4) is a specially programmed IC that controls the interrupts on the Signal Controller board. There are seven priority levels of interrupts on the Signal Controller. The highest level is $\overline{\text{INT7}}$ (U4,2) and the lowest is $\overline{\text{INT1}}$ (U4,8). IC (U4) monitors these seven interrupts. When one occurs, it assigns the interrupt a 3-bit code and outputs it to the microprocessor on $\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$ and $\overline{\text{IPL2}}$. When the microprocessor recognizes this interrupt, it responds by setting FC0, FC1, and FC2 high. IC (U4) then completes the handshake by pulling $\overline{\text{VPA}}$ low. When the software that services that interrupt is run, the interrupt is cleared and $\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL2}}$ and $\overline{\text{VPA}}$ go inactive high. If a second interrupt occurs at the same time as the first, and if it has a higher priority, the 3-bit code of the second interrupt is sent to the microprocessor, even though the

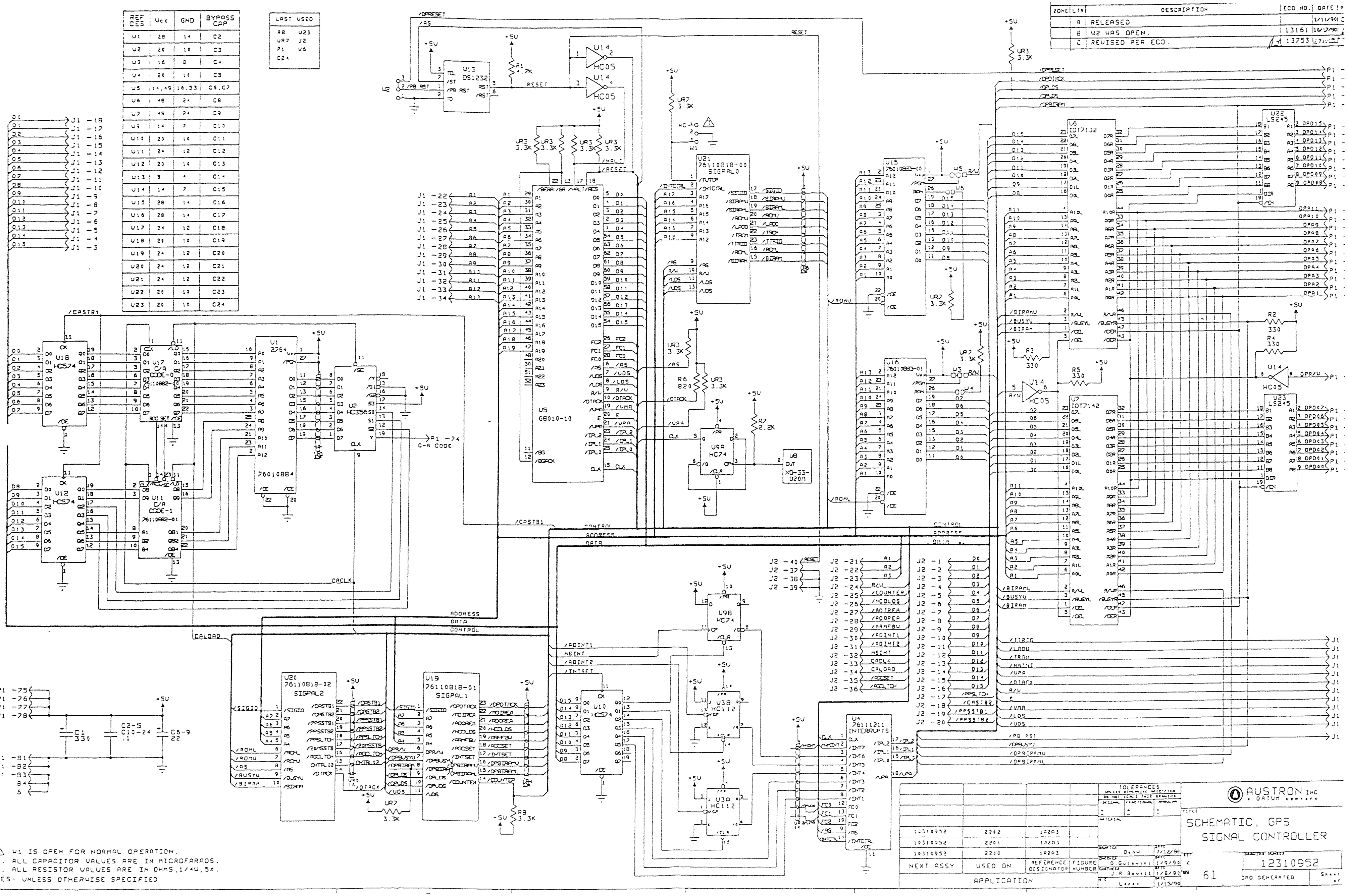
first has not yet been serviced. If a second interrupt of lower priority occurs, its code will not be placed on the bus until the higher priority interrupt has been cleared.

Latches (U9) and (U3) latch the occurrence of interrupts MSINT (interrupt every millisecond), ADINT1 (first A/D interrupt) and ADINT2 (second A/D interrupt). When these interrupts are serviced, the microprocessor clears the appropriate flip-flop by writing a zero into the proper bit of latch (U10). The corresponding output of (U10) goes to the reset input of the flip-flop that latched the interrupt. The bit is then set high, to allow another interrupt (it can also be left low to inhibit interrupts).

ICs (U19), (U20) and (U21) are specially programmed to decode the microprocessor address lines, various microprocessor control lines and other signals, to generate several device enable strobes. On the schematic, the inputs are shown on the left side of the logic block and the outputs are shown on the right. Each IC produces its own set of strobes, controlling particular parts of the hardware.

The circuit consisting of (U1), (U2), (U11), (U12), (U17) and (U18) produces the C/A code for each of the satellites being tracked. A 10-bit counter in (U11) and (U17) counts continuously from 0000 to 1022, strobing the lower 10 address lines of EPROM (U1). EPROM (U1) is programmed with all of the possible C/A codes. With each new count, a new byte in the EPROM is accessed and sent to the inputs of multiplexer (U2). Three outputs from latch (U12) (pins 17, 16, 15) are set by the microprocessor and are connected to the select inputs, S0-S2, of (U2). The 3-bit code on these lines selects one of the bits of the 8-bit byte coming from the EPROM. As the 10-bit counter increments, a sequence of ONEs and ZEROs appears at pin 19 of (U2).

By changing the three select lines of (U2), eight different C/A codes can be accessed in this way. Three additional control lines, (U12,14), (U12,13) and (U12,12), control the three most significant address lines of the EPROM. These three lines can be coded to access eight different blocks of memory in the EPROM. This means that eight blocks of the EPROM contain eight different C/A code sequences, giving a total of 64 possible 1023-bit codes.



REF DES	Vcc	GND	BYPASS CAP
U1	28	14	C2
U2	20	10	C3
U3	16	8	C4
U4	20	10	C5
U5	14,49	16,53	C6,C7
U6	48	24	C8
U7	48	24	C9
U9	14	7	C10
U10	20	10	C11
U11	24	12	C12
U12	20	10	C13
U13	8	4	C14
U14	14	7	C15
U15	28	14	C16
U16	28	14	C17
U17	24	12	C18
U18	20	10	C19
U19	24	12	C20
U20	24	12	C21
U21	24	12	C22
U22	20	10	C23
U23	20	10	C24

LAST USED	
R8	U23
UR7	J2
P1	W6
C24	

ZONE	LTR	DESCRIPTION	ECO NO.	DATE
	A	RELEASED		1/11/90
	B	W2 WAS OPEN.	13161	10/2/90
	C	REVISED PER ECO.	13753	

3. W1 IS OPEN FOR NORMAL OPERATION.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
12310952	2202	1A2A3	
12310952	2201	1A2A3	
12310952	2200	1A2A3	

APPLICATION

AUSTRON INC
A DATUM COMPANY

SCHEMATIC, GPS
SIGNAL CONTROLLER

12310952

61

CAD GENERATED